DAEV

UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mark T. McCORMACK, *et al.*

Ser. No.: **09/866,092**

Filed: May 23, 2001

For: *Structure and Method of Embedding Components in Multi-Layer Substrates*

Examiner: Eugene LEE

Art Unit: 2815

Att'y. Dkt.: 02EK-104724

CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R. § 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

(X) deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

( ) transmitted by facsimile to the Patent and Trademark Office.

4-7-05
Date

Jordan Wilson

PETITION TO CORRECT TYPOGRAPHICAL ERROR

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On February 4, 2005, the undersigned filed a "Request for Continued Examination," a "Petition for Extension of Time" and an "Amendment 'D'" (collectively, the "RCE Documents") with the United States Patent and Trademark Office ("USPTO") for the above application in response to the final Office Action dated October 5, 2004. Unfortunately, the Serial Number indicated on each of the RCE Documents contained a typographical error. The correct Serial Number for RCE Documents is 09/866,092 and **not** 09/886,092. Because of this typographical error, it appears that none of the RCE Documents were entered into the correct file.

Attached is a return postcard stamped by the USPTO showing that the RCE Documents were received by the USPTO on February 7, 2005. Applicant has also confirmed that the check which accompanied the RCE Documents, in an amount to cover the fees for the Request for Continued Examination and Petition for Extension of Time, has been cashed by the USPTO.

The undersigned learned of this error on April 6, 2005, when the examiner called to inquire whether applicant intended to abandon the application. In discussing the matter with the Examiner, he indicated that applicant should this Petition. He further indicated that the case would not be listed as abandoned.

Applicant respectfully petitions: (1) that the typographical error be corrected and (2) that the documents accepted as filed in Application Serial Number 09/866,092 either as of February 4, 2005 (the date on the Certificate of Mailing) or February 7, 2005, (the date the documents were actually received by the USPTO). A duplicate copy of the RCE documents accompany this Petition.

This Petition is accompanied by a petition fee in the amount of $130.00 as set forth in 37 C.F.R. § 1.17(h). The Commissioner is hereby authorized to charge any additional fees which may be required in this application under 37 C.F.R. §§ 1.16-1.17 or credit any overpayment, to Deposit Account No. 501395. This sheet is filed in duplicate.

April 6, 2005

Respectfully submitted,

Sheppard Mullin Richter & Hampton LLP
Four Embarcadero Center, 17th Floor
San Francisco, CA 94111-4106
Tel: (415) 774-3208
Fax: (415) 434-3947

David Schnapf
Registration No. 31,566

McCormack, *et al.*
6136-54242 (25916-217)
Serial No.: **09/866,092**
VIA U.S. FIRST CLASS MAIL

February 4, 2005
DS:jw
Filed: May 23, 2001

Title: STRUCTURE AND METHOD OF EMBEDDING COMPONENTS IN MULTI-LAYER SUBSTRATES

Enclosed:

1. Request for Continued Examination (in duplicate).
2. Petition for Extension of Time (1-mo. – in duplicate).
2 Amendment Transmittal (in duplicate).
3. Amendment "D" (13 pgs.).
4. Check No. 027188 for 910.
5. Return postcard.

Please acknowledge receipt by stamping and returning.
Thank You – Sheppard Mullin Richter & Hampton LLP

02EK-104724

PTO/SB/30 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	09/886,092
Filing Date	May 23, 2001
First Named Inventor	Mark T. McCormack
Art Unit	2815
Examiner Name	Eugene Lee
Attorney Docket Number	02EK-104724

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☑ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 501395. I have enclosed a duplicate copy of this sheet.

      i. ☐ RCE fee required under 37 CFR 1.17(e)

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☑ Other Charge any additional fees -or- credit any overpayments.

   b. ☑ Check in the amount of $ 910.00 enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	2/4/05
Name (Print/Type)	David Schnapf	Registration No.	31,566

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature			
Name (Print/Type)	Jordan Wilson	Date	2/4/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Mark T. McCORMACK, *et al.*

Serial No.: **09/886,092**

Filed: May 23, 2001

For: *Structure and Method of Embedding Components in Multi-Layer Substrates*

Examiner: Eugene LEE

Art Unit: **2815**

Att'y Dkt.: 02EK-104724

CERTIFICATE OF MAILING/TRANSMISSION
(37 C.F.R. § 1.8A)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

2/4/05 Jordan Wilson
Date

AMENDMENT TRANSMITTAL

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing is an amendment/response in the above-identified application.

FEE CALCULATION FOR CLAIMS AS AMENDED

	As Amended		Previously Paid For		Present Extra	Rate	Additional Fee
Independent Claims	3	-	3	=	0	$ 86.00	$0.00
Total Claims	26	-	35	=	0	$ 18.00	$0.00
For Multiple Dependent Claims	0		0			$290.00	$0.00
					Total Additional Fee:		**$0.00**

( ) Small Entity Fee (reduced by half).

(X) No additional claim fee is required.

( ) A check in the amount of _____ is enclosed.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required in this application under 37 C.F.R. §§1.16-1.17 or credit any overpayment, to Deposit Account No. **501395**. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Assistant Commissioner is authorized to charge the unpaid amount to Deposit Account No. **501395**. This sheet is filed in duplicate.

February 4, 2005

Respectfully submitted,

Sheppard Mullin Richter & Hampton LLP
4 Embarcadero Center, 17th Floor
San Francisco, CA 94111-4106
Tel: (415) 434-9100
Fax: (415) 434-3947

David Schnapf
Registration No. 31,566

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mark T. McCORMACK, et al.
Ser. No.:	09/886,092
Filed:	May 23, 2001
For:	*Structure and Method of Embedding Components in Multi-Layer Substrates*
Examiner:	Eugene LEE
Art Unit:	2815
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Mail Stop RCE
Commissioner for Patents
P.O. Box 1450,
Alexandria, VA 22313-1450

2/4/05 Jordan Wilson
Date

PETITION FOR EXTENSION OF TIME

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant(s) hereby petition(s) under 37 C.F.R. §1.136(a) for an extension of time for response in the above identified application for the period required to make the accompanying response timely, or, if there be no accompanying response, for the period for which the fee is indicated.

Extension fee for response within first month:

( ) By a small entity $60.00
(X) By other than a small entity $120.00

Extension fee for response within second month:

( ) By a small entity $225.00
( ) By other than a small entity $450.00

Extension fee for response within third month:

( ) By a small entity $510.00
( ) By other than a small entity $1020.00

(X) A check in the amount of **$910.00** is enclosed herewith which includes the extension fee of **$120.00** and the RCE fee of **$790.00**.

( ) Charge $_____ to Deposit Account No. 501395.

The Commissioner is hereby authorized to charge any additional fees which may be required in this application under 37 C.F.R. §§ 1.16-1.17 or credit any overpayment, to Deposit Account No. 501395. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 501395. (This sheet is filed in duplicate.)

February 4, 2005

SHEPPARD MULLIN RICHTER & HAMPTON LLP
Four Embarcadero Center, 17th Floor
San Francisco, CA 94111-4106
Telephone: (415) 434-9100

By: _____
David Schnapf
Registration No. 31,566

UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mark T. McCORMACK, *et al.*

Ser. No.: **09/886,092**

Filed: May 23, 2001

For: *Structure and Method of Embedding Components in Multi-Layer Substrates*

Examiner: Eugene LEE

Art Unit: 2815

Att'y Dkt.: 02EK-104724

CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R. § 1.8A)

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P.O. Box 1450
Alexandria, VA 22313-1450

( ) transmitted by facsimile to the Patent and Trademark Office.

2/4/05 Jordan Wilson

Date Jordan Wilson

AMENDMENT "D"

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This amendment is submitted under 37 C.F.R. § 1.114 in connection with the filing of a Request for Continued Examination ("RCE") responsive to the "final" Office Action dated October 5, 2004. Withdrawal of the finality of the Office Action and entry and consideration of these amendments and remarks are respectfully requested pursuant to § 1.114(d).

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 7 of this paper.

The USPTO is requested to update the "Attorney Docket Number" for this case. The new docket number, listed above, is **02EK-104724**.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

Claims 1 – 16 (cancelled).

Claim 17 (currently amended). A multi-layer printed circuit board having at least one prefabricated integrated electronic component embedded therein comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board and having a first substrate surface and a second substrate surface;

a first integrated electronic component, where said first integrated electronic component is prefabricated prior to being ~~secured~~ securely attached in a cavity in said first substrate surface;

~~an adhesive securing said first prefabricated integrated electronic component within said first substrate surface cavity;~~

a first dielectric layer disposed on said first substrate surface and over said first integrated electronic component;

a metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said metallic layer; and

a second dielectric layer disposed over said first via and over said metallic layer,

a second electrically conductive via extending through said first and second dielectric layers and electrically coupled to said first integrated electronic component.

Claim 18 (previously presented). The multi-layer printed circuit board of Claim 17 additionally comprising a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface.

Claim 19 (currently amended). The multilayer printed circuit board of Claim 17 wherein said circuit board substrate comprises a multi-layer core substrate comprising at least two polymeric layers.

Claim 20 (previously presented). The multilayer printed circuit board of Claim 17 wherein said first via extends from said first substrate surface to said second substrate surface.

Claim 21 (previously presented). The multilayer printed circuit board of Claim 18 wherein said first via extends from said first substrate surface to said second substrate surface.

Claim 22 (currently amended). The multilayer printed circuit board of Claim 18 wherein said first metallic layer is patterned to expose ~~at least~~ a portion of said first substrate surface, and said cavity is formed in the exposed portion of said first substrate surface ~~and said first prefabricated integrated electronic component is secured within said cavity in said exposed portion of said first substrate surface~~.

Claim 23 (currently amended). The multilayer printed circuit board of Claim 18 wherein said second metallic layer is patterned to expose ~~at least~~ a portion of said second substrate surface.

Claim 24 (original). The multilayer printed circuit board of Claim 23 additionally comprising a second integrated electronic component secured to said exposed portion of said second substrate surface.

Claim 25 (cancelled).

Claim 26 (currently amended). The multilayer printed circuit board of Claim 24 ~~25 additionally comprising a~~ wherein said second integrated electronic component is disposed in ~~said~~ a cavity formed in said exposed portion of said second substrate surface.

Claim 27 (currently amended). The multilayer printed circuit board of Claim 18 ~~17~~ wherein said first prefabricated integrated electronic component comprises a conductive pad contacting said first metallic layer.

Claim 28 (currently amended). The multilayer printed circuit board of Claim 24 ~~25 additionally comprising~~ wherein said ~~first prefabricated~~ second integrated electronic component comprises a conductive pad contacting said second metallic layer.

Claim 29 (currently amended). The multilayer printed circuit board of Claim 26 ~~additionally comprising~~ wherein said first prefabricated integrated electronic component comprises a conductive pad contacting said first metallic layer.

Claim 30 (original). The multilayer printed circuit board of Claim 17 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 31 (currently amended). The multilayer printed circuit board of Claim ~~25~~ 24 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 32 (original). The multilayer printed circuit board of Claim 26 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 33 (original). The multilayer printed circuit board of Claim 27 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 34 (original). The multilayer printed circuit board of Claim 33 additionally comprising a patterned metal layer disposed on said second dielectric layer.

Claim 35 (cancelled).

Claim 36 (new). The multilayer printed circuit board of Claim 17 wherein said first prefabricated integrated electronic component is a capacitor.

Claim 37 (new). The multilayer printed circuit board of Claim 36 wherein said capacitor comprises a petrovskite capacitance material.

Claim 38 (new). The multilayer printed circuit board of Claim 17 wherein said first prefabricated integrated electronic component is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board.

Claim 39 (new). The multilayer printed circuit board of Claim 38 wherein said first prefabricated integrated electronic component is fabricated at a temperature of greater than about 600°C.

Claim 40 (new). A multi-layer printed circuit board comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board;

a prefabricated capacitor disposed in a cavity in said substrate, said capacitor having a contact pad;

a first dielectric layer disposed on said substrate and over said capacitor;

a metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said contact pad; and

a second dielectric layer disposed over said first via and over said metallic layer,

a second electrically conductive via extending through said first and second dielectric layers and electrically coupled to said capacitor.

Claim 41 (new). The multi-layer printed circuit board of claim 40, comprising a plurality of cavities and a plurality of capacitors.

Claim 42 (new). The multi-layer printed circuit board of claim 40 wherein said capacitor comprises a petrovskite capacitance material.

Claim 43 (new). The multi-layer printed circuit board of claim 40 wherein said capacitor is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board.

Claim 44 (new). A multi-layer printed circuit board comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board, said substrate having opposing first and second sides;

a prefabricated electronic component disposed in a cavity formed in said first side of said substrate, said prefabricated electronic component having a contact pad;

a first dielectric layer disposed on said first side of said substrate and over said prefabricated electronic component;

a patterned metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said contact pad;

a second dielectric layer disposed over said first via and over said metallic layer;

a second electrically conductive via extending through said first and second dielectric layers;

a third dielectric layer disposed on said second side of said substrate; and

a patterned metallic layer disposed on said third dielectric layer.

REMARKS

This Amendment, which is timely with the accompanying Petition for Extension of Time, is submitted in connection with a Request for Continued Examination under 35 U.S.C. § 132(b) and 37 C.F.R. § 1.114, responsive to the "final" Office Action mailed October 5, 2004. In the Office Action all of the pending claims, namely claims 17 – 34, were rejected under 35 U.S.C. §§ 102 and 103 as being anticipated by or obvious in view of various prior art references, discussed below. Claims 28 and 29 were also objected to due to minor informalities. In addition, the drawings were objected to under 37 C.F.R. § 1.83(a). By this amendment, claims 17, 19, 22, 26, 27, 28, 29 and 31 have been amended to overcome the rejections, to improve clarity and to correct the informalities noted by the examiner. In addition, claim 25 has been cancelled and new claims 36 – 44 have been added. Claims 1 – 16 and 35 were previously cancelled. Thus, claims 17 – 24, 26 – 34 and 36 – 44 are pending. Continued examination under 37 C.F.R. § 1.114 is respectfully requested.

Drawing Objections

The drawings were objected to as failing to show every feature of the invention specified in the claims. This application has now seen four Office Actions, and applicant fails to understand why none of these drawing objections were raised in the prior Office Action. The examiner is reminded of 37 C.F.R. § 1.104 which requires that the examiner's Office Action be "complete" and MPEP § 707.07(g) which requires avoidance of piecemeal examination.

Three specific objections were raised, which are discussed in order:

(1) Failure to show an adhesive securing the prefabricated integrated electronic component. As discussed below, claim 17 has been amended to delete the requirement of an adhesive. Therefore, this objection is now moot.

(2) Failure to show the first integrated electronic component within said first substrate cavity. The examiner concedes that FIG. 13 shows the first integrated electronic component within the first substrate cavity, but notes that FIG. 13 does not show the entirety of what is recited in claim 17. (FIGS. 14 and 15 also show core structures with prefabricated electronic components disposed in cavities.) Apparently, it is the examiner's position that all of the features of the claimed invention must be shown in the same figure. There is no such legal

requirement. Therefore, this objection is ***traversed*** because all of the features of claim 17 are shown in the drawings, which is all that is required. It is extremely commonplace for different aspects of an invention to shown in different drawing figures. Here, the application clearly states that the core structure depicted in FIG. 13 (or FIG. 14 or FIG. 15) can be substituted for the core structure shown in FIG. 9. See, *e.g.*, page 7, last paragraph.

(3) Failure to show that the exposed portion of the second substrate surface has a cavity. This same objection was initially made in the Office Action dated December 17, 2002. In response, in Amendment "A", applicant pointed out that FIG. 12 shows a cavity. In addition, Amendment "A" provided a new FIG. 13 which shows a component in the cavity. The examiner reiterated this drawing objection in the Office Action dated August 19, 2003, without further explanation, but presumably because none of the figures showed a substrate with cavities on *both* sides. Thereafter, in its Amendment "B", applicant added a new FIG. 15 which shows a core substrate having cavities on *both* sides thereof. The examiner then **dropped** this objection, presumably because applicant's new FIG. 15 clearly shows the claimed feature. Accordingly, this objection is ***traversed*** because FIG. 15 clearly shows a core substrate having cavities with components on both sides thereof. It is noted, that this objection makes reference only to claim 25, which has now been cancelled. Thus, it appears that the objection may also be moot.

In view of the foregoing, applicant submits that no further drawing amendments are required.

Claim Amendments and Additions

In view of the drawing objection, described above, claim 17 has been amended to delete the recitation of an adhesive for securing the prefabricated component in the cavity. It is believed that inclusion of the adhesive is not necessary to the patentability of the claim. This element was added to provide a structural difference between the previously cited prior art, wherein electronic components were created *in situ*. It no longer appears necessary to include this claim element to differentiate over the prior art and, therefore, it has been dropped.

Claim 17 has also been amended to specify that the core substrate is a polymeric substrate. This has been added to distinguish the present invention over the prior, as discussed in greater detail below. Support for this is found in the specification, as filed, on page 10, first

paragraph, which states: "Suitable dielectric material for the core 12 ... include B-stage polymeric compounds ..." and then goes on to list a large variety of suitable polymers.

Claim 19 has been amended to recite that the multilayer core substrate comprises at least two *polymeric* layers.

Claims 22 and 23 have been amended to improve the wording thereof. Since the metallic layer is "patterned" it inherently does not cover the entire surface of the substrate – *i.e.*, the fact that a portion is "exposed" is inherent. Therefore, the words "at least" do not add anything to the claims and this phrase has been dropped. Applicant would like the record to be clear that the term "exposed," as used herein, denotes the fact that after a metallic layer is patterned (*i.e.*, a portion of the metal is removed), the substrate surface which was once covered with metal is again exposed. Thereafter, in accordance with the present invention, the "exposed" portion may be covered by other layers so that, in a sense, it is no longer "exposed." Nonetheless, it would be clear to those skilled in the art that the phrase "exposed portion" means that portion of a layer which is removed during patterning, notwithstanding the fact that such portion may later be covered.

Claim 26 has been amended to provide greater clarity, and to change the dependency in view of the cancellation of claim 25.

Claims 28 and 29 have been amended to correct the informalities noted by the examiner. In addition, the dependency of claim 28 has been changed in view of the cancellation of claim 25.

Claim 31 has been amended to change the dependency in view of the cancellation of claim 25.

New claims 36 – 44 have been added. Claims 40 and 44 are in independent form to provide independent claims of varying scope. The patentability of these claims is discussed below.

Claims 36, 37 and 40 – 43 all specify that the prefabricated component is a capacitor. Support for this limitation is found, *inter alia,* in the Specification, as originally filed, on page 7, last paragraph, page 8, first paragraph, and page 10, last paragraph.

Claims 37 and 42 add the requirement that the capacitor comprises a petrovskite capacitance material. Support for this limitation is found, *inter alia,* in the Specification, as originally filed, on page 8, first paragraph and page 10, last paragraph.

Claims 38, 39 and 43 add the requirement that the prefabricated component is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board, with claim 39 specifying that the component is fabricated at a temperature greater than 600°C. Support for these limitations is found in the paragraph bridging pages 10 and 11 of the application, as originally filed.

Traversal Of Claim Rejections

Anticipation

Claims 17 – 23, 27 and 30 were rejected as anticipated by Miura et al., U.S. Pat. No. 5,565,706, ("Miura"). Miura is believed to be more pertinent than the previously cited prior art. Independent claim 17 has been amended to specify that the core substrate is "polymeric." Support for this amendment is discussed above. ALL of the embodiments discussed in Miura use ceramic or silicon core substrates. This is true notwithstanding the fact that the patent discloses the use of polymers for other purposes. It is further noted that the one embodiment which uses a silicon core substrate does NOT form a cavity in the silicon substrate – in fact FIG. 11 does not show any devices mounted on the silicon, presumably, as stated in the patent, because silicon is susceptible to warping.

Since Miura does not disclose the use of a polymeric core substrate, it does not anticipate claim 17, as amended, or any of the other pending claims (including the newly added claims), all of which include this requirement.

Nor would it be obvious to substitute the polymeric core substrate of the present invention for Miura's ceramic core substrates. Miura carefully and consistently differentiates ceramic substrates from polymeric substrates. Thus, for example, it contains an extended discussion under the heading, "Description of the Related Art," differentiating ceramic wiring boards and polymeric wiring boards. It is clear from this discussion that the two are not considered interchangeable. One important difference between ceramic and polymeric substrates is their respective thickness. The ceramic substrates disclosed in Miura are 0.8 mm (800

microns) thick, whereas the polymeric layers disclosed in the patent are 40 microns thick – *i.e.*, 5% of the ceramic substrate thickness. Thus, there is no reason why someone skilled in the art would be motivated to replace the ceramic substrate of Miura with a polymeric substrate.

Regarding claim 18, Miura does not disclose a metallic layer on the *second* substrate surface (*i.e.*, on the bottom surface of the substrate). The examiner refers to layer 8, but this is over the first substrate layer, not the second substrate layer. Claims 21 – 24, 26 – 29, 31 and 32 are all dependent on claim 18 and are allowable for the same reason.

Regarding claim 19, as amended, Miura does not suggest a core substrate comprising at two polymeric layers. Indeed, Miura does not show or suggest a multilayer core substrate of any sort. The examiner offered no explanation of how Miura reads on claim 19.

Regarding claim 23, as amended, which is dependent on claim 18, Miura does not disclose a patterned metallic layer on the bottom of the substrate. The examiner offered no explanation of how Miura reads on claim 23.

Regarding claims 24 and 26, Miura does not disclose a core substrate having prefabricated electronic components mounted on both sides thereof. The examiner offered no explanation of how Miura reads on claims 24 or 26. In numbered paragraph 6 of the Office Action (pages 4 – 5), the examiner admits that "Miura does not disclose said exposed portion of said second substrate including a cavity additionally comprising a second integrated electronic component disposed in said cavity." Thus, the examiner concedes that Miura does not anticipate these claims and, therefore, his § 102 rejection is inexplicable.

All of the new claims also contain the limitation that the core substrate is polymeric and, therefore, none of them are anticipated by Miura. Moreover, new claims 36, 37 and 40 – 43 are all directed to structures with prefabricated capacitors. This is not shown in Miura which, therefore, does not anticipate these claims for that additional reason. New claims 38, 39 and 43 all require that the prefabricated component undergo high temperature processing. This is not disclosed in Miura.

Obviousness

Claims 24 – 26, 28, 29, 31 and 32 were rejected under 35 U.S.C. § 103 as being "obvious" over Miura in view of Wojnarowski et al., U.S. Pat. No. 5,703,400 ("Wojnarowski"). Applicant respectfully traverses this rejection.

Wojnarowski discloses forming a chip module by mounting a IC chip on a flexible substrate. Two such substrates may then be sandwiched together, in face-to-face fashion, and a molding material injected into the space between the substrates to join them by encapsulation. This is an entirely different structure made by an entirely different process than anything disclosed in the present invention or in Miura. Wojnarowski does not really have a core substrate, as required by the claims of the present application. The structures are fully formed before they are molded together by an encapsulant. Moreover, Wojnarowski's structure is incompatible with the ceramic core substrate of Miura, and uses entirely different processing techniques. Thus, the examiner's explanation of why someone skilled in the art would be motivated to modify Miura in view of the teachings of Wojnarowski is not well founded. In any case, even if someone were motivated to modify the structure of Miura to use cavities on both sides of the substrate, there would be no reason to change from a ceramic core substrate, as this feature is central to the teachings of Miura. Thus, there would be no reason to use a polymeric core as per the amended claims. Accordingly, it is submitted that there would be no motivation to combine the references, and even when they are combined they do not make the present invention obvious.

Claims 33 and 34 were rejected as being obvious over Miura in view of Ma et al., U.S. Pat. No. 6,154,366 ("Ma"). Ma merely shows an IC chip which is mounted on a flexible wiring interconnect, referred to in the patent as a "flex component." The chip is then encapsulated with an encapsulant, and additional wiring layers may be added onto the flex component. Ma is principally directed to the use of moisture barriers surrounding the chip. Ma does not show a cavity formed in a core substrate in which a prefabricated component is mounted. In this regard, surrounding a component that has already be connected to a substrate with an encapsulating material is much different than securing a prefabricated component in a cavity that has been pre-formed in a substrate. Thus, the structure described in Ma is much different than the structure of Miura and it is submitted that there is no reason why one of ordinary skill in the art would be motivated to combine the teachings of these vastly different references which are directed to solving vastly different problems. Accordingly, applicant respectfully submits that the combination asserted by the examiner does not make claims 33 or 34 obvious.

New claims 36, 37 and 40 – 43 all required that prefabricated capacitors be incorporated into cavities formed in polymeric core substrates. None of the prior art of record relied upon by the examiner shows capacitors secured in cavities in polymeric substrates. Claims 37 and 42 further specify that the capacitors comprise a petrovskite capacitance material. No such material is discussed in any of the references relied upon by the examiner.

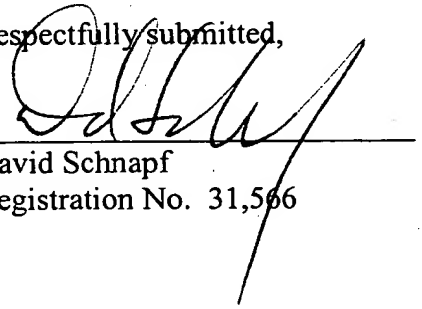
Claims 38, 39 and 43 specify that the component/capacitor is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board, with claim 39 specifying a minimum processing temperature. These limitations are not disclosed in or made obvious by the references of record.

Conclusion

In view of the amendments and remarks made above, applicant respectfully submits that the application is in condition for allowance and action to that end is respectfully solicited. The examiner is invited to telephone the undersigned at the number listed below if it is believed that a telephone interview would advance the prosecution of this matter.

February 4, 2005

Respectfully submitted,



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